Mechanically Flexible Interconnects With Contact Tip for Rematable Heterogeneous System Integration

Chaoqi Zhang, Hyung Suk Yang, Hiren D. Thacker, Ivan Shubin, John E. Cunningham, and Muhannad S. Bakir, *Senior Member, IEEE*

***Abstract*— A wafer-level, batch-fabricated, mechanically flexible interconnect (MFI) with a contact tip has been developed for rematable heterogeneous system integration. The contact tip, which exhibits a truncated-cone profile, enhances the scrubbing capability while maintaining the tip lifetime by avoiding tip plastic deformation. Electrical and mechanical characterization has been conducted on various testbeds to verify the performance of the assembled chip links with MFIs. The results indicate that a single MFI has an average electrical resistance of 103.21 mΩ and up to 1 A current carrying capability, and can be successfully assembled on nonplanar surfaces with up to 45-μm surface variation.**

***Index Terms*— Advanced packaging, flexible interconnect, heterogeneous integration, NiW, rematable assembly.**

I. Introduction

HETEROGENEOUS chip integration has been investigated for many decades and has emerged as a promising approach to realize large-scale, high-performance computing systems [1]–[8]. However, as the number and diversity of integrated chips increase, the cost and yield of a heterogeneous system suffer from the increased complexity of system-level testability. In addition, since chips are typically permanently soldered, there is a lack of repairability, which can increase system cost. Moreover, yields on reworkability could be substantially improved over current industry standard practices.

We propose a novel integration platform in which solder joints are replaced with flexible interconnects to alleviate system-level testability and repairability, as shown in Fig. 1. To realize this rematable heterogeneous integration platform, the flexible interconnects need to exhibit the following characteristics: 1) relatively large bending force for reliable contact; 2) large vertical range of motion to overcome substrate warpage and topological variation; 3) low electrical contact resistance; 4) long lifetime; and 5) low-cost wafer-level batch fabrication process. However, due to limitations stemming from material property, design, and/or fabrication processes, it is challenging for traditional flexible interconnect technologies [9]–[21] to meet the requirements above. We previously reported Au–NiW-based mechanically flexible interconnects (MFIs) [22]–[26] as a promising rematable interconnect technology for various applications [27]–[32]. In this paper, the Au–NiW-based MFIs have been advanced by adding a contact tip. The tip structures on previously reported flexible interconnects were designed to be suitable for permanent solder attachment [12], [18], [21]. In this paper, the contact tip is designed with a truncated-cone shape for enhanced rematable interconnection. Various testbeds consisting of chips with MFIs and corresponding substrates were assembled to demonstrate the electrical and mechanical performance of the MFIs.

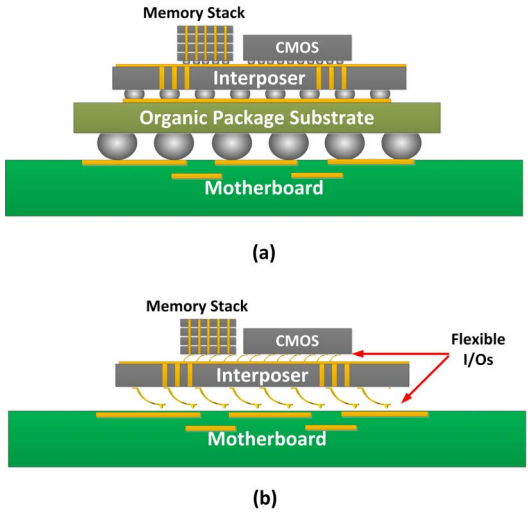

Fig. 1. (a) Traditional 2.5-D heterogeneous system. (b) Rematable 2.5-D system enabled using MFIs.

The fabrication and experimental design of the MFI technology under consideration is discussed in Section II. Rematable chip assembly using MFIs is demonstrated and characterized in Section III. In Section IV, robust assembly of a silicon chip on a nonplanar surface using MFIs is reported. Finally, Section V presents the conclusion.

II. Experimental Design and Fabrication Process

In this section, the fabrication of Au–NiW MFIs with a truncated-cone tip is discussed first. Next, the testbed design, fabrication, and results are described.

Manuscript received March 19, 2016; revised July 21, 2016; accepted September 1, 2016. Date of publication October 26, 2016; date of current version November 7, 2016. Recommended for publication by Associate Editor T.-C. Chiu upon evaluation of reviewers' comments.

C. Zhang, H. S. Yang, and M. S. Bakir are with the Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: chqzhang@gatech.edu).

H. D. Thacker, I. Shubin, and J. E. Cunningham are with Oracle Corporation, San Diego, CA 92121 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCPMT.2016.2614997

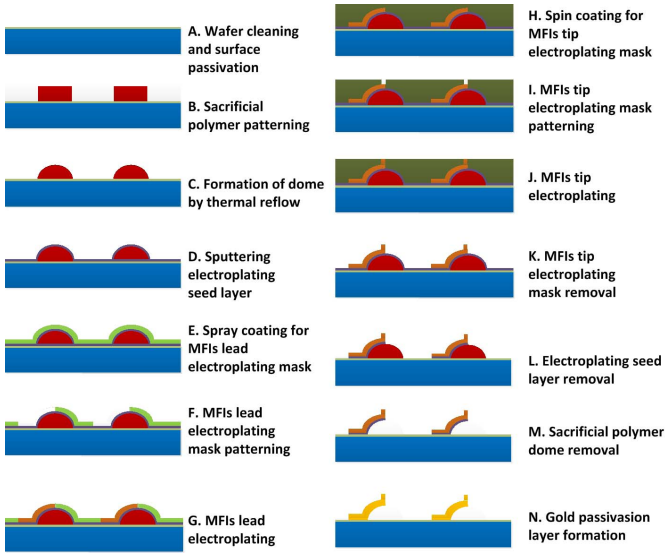

Fig. 2. Fabrication process of MFIs with a truncated-cone tip.

A. Fabrication of MFIs With Truncated-Cone Tip

Based on our previously reported Au–NiW MFIs [22]–[26], the fabrication process of Au–NiW MFIs with a contact tip is developed and is shown in Fig. 2. The fabrication process of the MFIs begins with the formation of a sacrificial polymer dome accomplished by patterning and thermally reflowing a spin-coated polymer layer on a nitride-passivated silicon wafer. Next, a Ti/Cu/Ti film was sputtered on top of the 65-μm-tall polymer domes as an electroplating seed layer. Following seed layer formation, a 12-μm-thick conformal photoresist layer was spray-coated and patterned on top of the seed layer as an electroplating mold [26]. After electroplating of the MFIs, the photoresist plating mold was removed, followed by patterning of another spin-coated photoresist for tip electroplating. Following tip formation, the tip electroplating mold, the seed layer, and the polymer domes were stripped, leaving behind MFIs with a truncated-cone tip and a 65-μm-high vertical gap above the substrate. Finally, the free-standing NiW MFIs on the test chip are passivated by a 0.3-μm-thick electroless plated gold finish.

An array of Au–NiW MFIs with a truncated-cone tip is shown in Fig. 3. As reported in [26], compared to the sputtering method, electroless gold plating does not require extra lithography steps and covers the entire surface area of the free-standing MFIs. The very thin (approximately 0.3 μm) Au passivation layer lowers the resistance and enhances the lifetime of the NiW MFIs while maintaining the desired mechanical properties [24]. In addition, during the assembly process, the Au–NiW MFIs form a low-contact resistance, in particular, to gold passivated bond pads.

SEM images of Au-NiW MFIs with a truncated-cone tip are shown in Fig. 4(a) and (b). The inline pitch of the fabricated MFIs is 150 μm, and they exhibit a standoff height of 65 μm. Accounting for the 10-μm-thick MFI and 30-μm-tall tip, the aggregate height of the fabricated MFI (anchor to tip) is approximately 105 μm, which is large enough to overcome

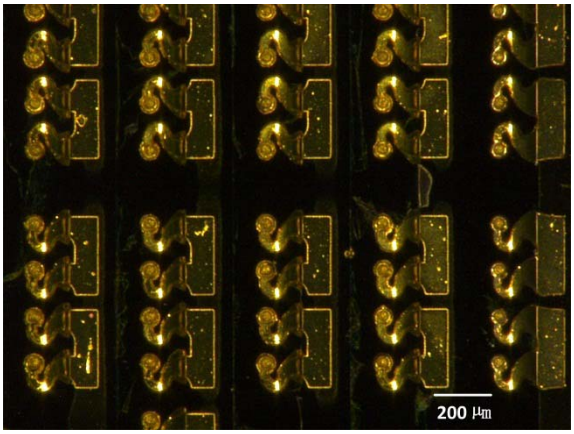

Fig. 3. MFIs with a truncated-cone tip after being passivated with a electroless gold layer.

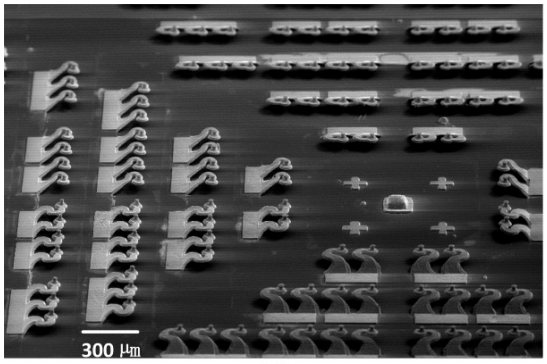

Fig. 4. (a) Array of free-standing Au-NiW MFIs with contact tip. (b) Au-NiW MFIs exhibit a 65-μm elastic vertical range of motion and a 30-μm-tall contact tip.

surface variation and warpage of organic substrates [33], as shown in Fig. 5. The contact tip was designed and fabricated as a truncated-cone shape for the following reasons: 1) the base of the tip is enlarged for better tip-to-lead adhesion and lower resistance; and 2) the contact tip can enhance the scrubbing to the bonding pads. The truncated-cone profile was formed by an electroplating process using a photoresist mold with a negative sidewall profile.

The pitch of the MFIs under consideration is compatible with the needs of advanced FCBGA (minimum pitch is approximately 150 μm). For higher density interconnects,

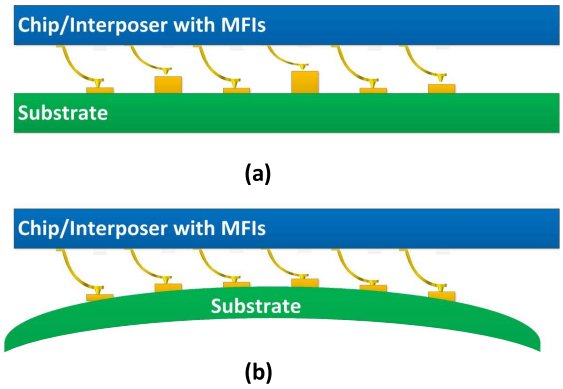

Fig. 5. (a) MFI enabled chip/interposer assembly on nonuniform substrates to demonstrate robust assembly and the ability of (b) the MFIs to compensate for nonplanar surfaces.

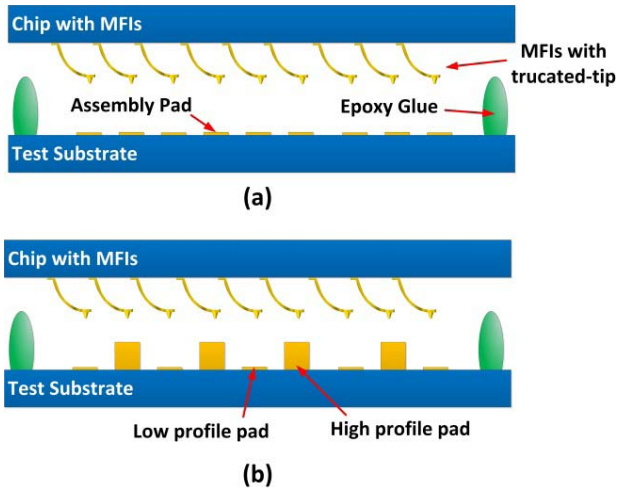

Fig. 6. Two investigated assembly experiments. (a) Assembly of a chip with MFIs onto a substrate with uniform-height pads multiple times for rematable assembly demonstration. (b) Assembly of a chip with MFIs onto a substrate with nonuniform-height pads to demonstrate the ability of the MFIs to compensate for nonplanar surfaces.

such as those used in the first-level interconnection, MFI pitch can be scaled, as demonstrated in [25]; MFIs with an inline pitch of 50 μm and 65 μm vertical gap were previously reported [26].

B. Experimental Design

Two types of assembly experiments were conducted to characterize the electrical and mechanical properties of the MFIs: 1) assembly of a chip with MFIs onto a substrate with uniform-height pads multiple times to demonstrate rematable assembly [Fig. 6(a)], and 2) assembly of a chip with MFIs onto a substrate with nonuniform-height pads to demonstrate robust assembly and the ability of the MFIs to compensate for nonplanar surfaces [Fig. 6(b)].

In both experiments, the chips were assembled using a Finetech submicrometer-resolution flip-chip bonder. Once aligned and mounted onto the substrate, the chips were affixed by applying epoxy to the corners of the chips. The applied force during the bonding process was calculated based on the

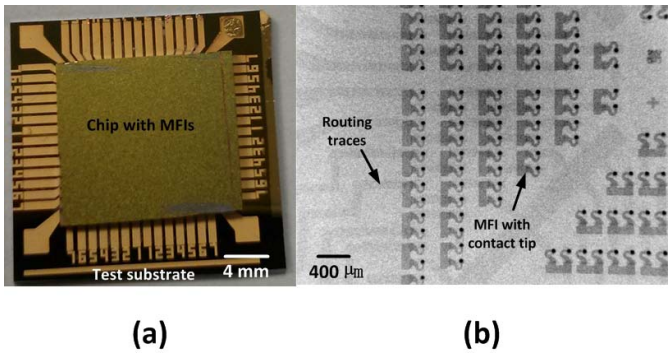

Fig. 7. (a) Optical image and (b) X-ray image of an assembled testbed.

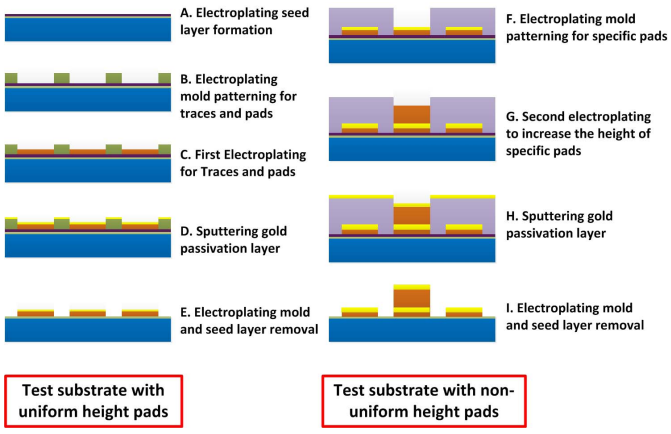

Fig. 8. Fabrication process of the test substrate with uniform-height pads (steps A–E) and the test substrate with nonuniform-height pads (steps F–I).

compliance, deformation depth, and number of MFIs on each chip. For the reported assembly, each chip contains 304 MFIs. Assuming each MFI has a compliance of 5 mm/N and will experience a deformation of 30 μm during assembly, the applied force during chip assembly is 1.82 N.

A sample assembled testbed is shown in Fig. 7(a). Following the assembly, an X-ray imaging tool, Dage X-Ray XD7600NT, was used to verify assembly alignment accuracy. The X-ray image shown in Fig. 7(b) illustrates not only the alignment accuracy but also the lack of any voids in the fabricated (electroplated) electrical links. In Fig. 7(b), the 3-μm-thick traces on the substrate are represented in the X-ray image by the light gray traces; the dark dots on top of the MFIs in the X-ray image are the truncated-cone tips.

C. Fabrication of the Test Substrate

Fig. 8 shows the fabrication processes of the two test substrates used in this paper. The fabrication of the substrate with uniform-height pads is shown in steps I–V: One lithography step was used to pattern the electroplating mold above a sputtered Ti/Cu/Ti seed layer; pads and traces were formed by Cu electroplating; next, a 300-nm-thick Au layer was sputtered as a passivation layer. Following the Au layer lift-off and seed layer removal, the substrate with uniform-height pads was obtained for the first set of assembly experiments [Fig. 6(a)]. For the assembly on nonuniform-height pads [Fig. 6(b)],

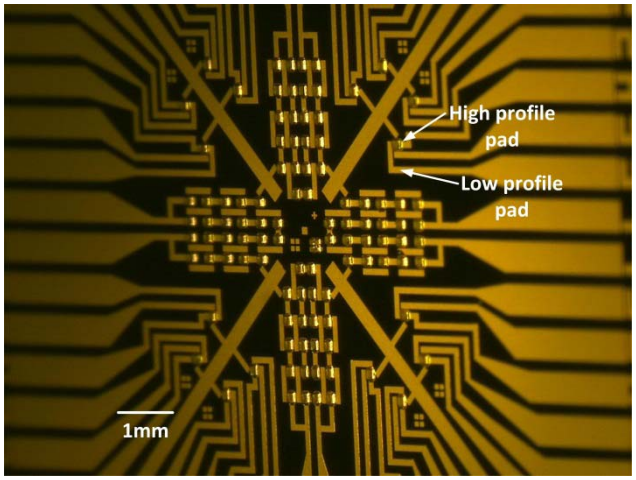

Fig. 9. Test substrate with nonuniform-height pads.

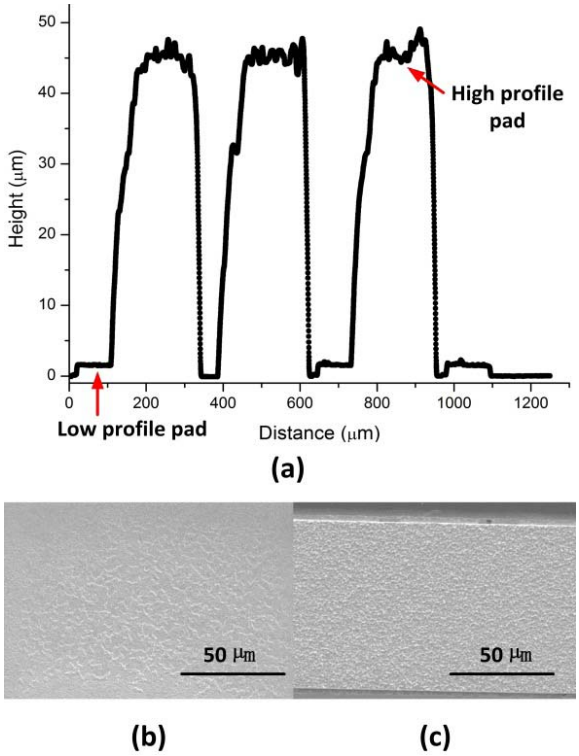

Fig. 10. (a) Surface profile of the test substrate with nonuniform pads. SEM images of the surface of (b) high-profile pad and (c) low-profile pad.

in addition to steps A–E, a second plating process was used to form the nonuniform-height pads (steps F–I).

Fig. 9 shows the test substrate with various-height pads. A surface topography scan using the Dektak 150 profilometer was performed to characterize the height of the pads across the substrate. As shown in Fig. 10(a), the low-profile pads are 3 μm tall and the high-profile pads are 48 μm tall, which leads to a 45-μm height difference. The surface roughness of the high-profile pads (approximately 5 μm) is much larger than that of the low-profile pads (approximately 1 μm) and was verified by SEM [SEM images of the surface of the high- and low-profile pads are shown in Fig. 10(b) and (c), respectively]. The rougher surface of the high-profile pads is believed to be caused by the higher deposition rate and the longer deposition time used in the second electroplating step. The impact of the surface roughness on the contact resistance will be discussed in Section IV.

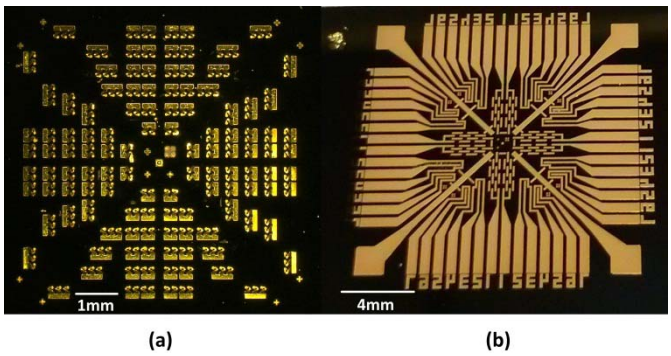

Fig. 11. Testbed with four-point resistance measurement structures, including (a) chip with MFIs and (b) corresponding substrate, is used for rematability verification.

III. MFIs-Assisted Rematable Assembly

In this section, the assembly experiment shown in Fig. 6(a) is used to demonstrate the rematable assembly of chips with truncated cone tip Au–NiW MFIs.

A. Rematability Verification

Four-point electrical measurements of the MFIs were performed using the testbed shown in Fig. 11. The rematability of the MFIs is demonstrated by comparing the four-point resistance measurement results of a testbed in which a chip was assembled once to that of a testbed in which a chip was mounted and remounted for a total of ten times.

Four-point resistance measurements were conducted using a Signatone Probe Station. A detailed schematic of the four-point resistance measurement setup is shown in Fig. 12(a). X-ray imaging, as shown in Fig. 12(b), was used to ensure the testing structure was aligned correctly. The measured resistance includes that of the MFI plus the contact resistance to the pad. The average resistance of 12 assembled samples is 103.21 mΩ, and the standard derivation is 4.06 mΩ.

To demonstrate the rematability, the testbed shown in Fig. 11 was repeatedly assembled for ten times and then measured using the four-point resistance setup described previously. The measured average resistance is 105.99 mΩ. As summarized in Table I, compared to the results from the testbed in which the chip was only mounted once, the difference in the resistance is negligible (less than 3 mΩ). SEM images were taken, as shown in Fig. 13, to verify that after repeated assembly, the Au–NiW MFIs maintain their original profile.

B. Yield and Current Carrying Capability Characterization

The yield and current carrying capability of the MFIs were performed on the testbed shown in Fig. 14. The chip and substrate were designed to form a daisy chain of serially interconnected MFIs.

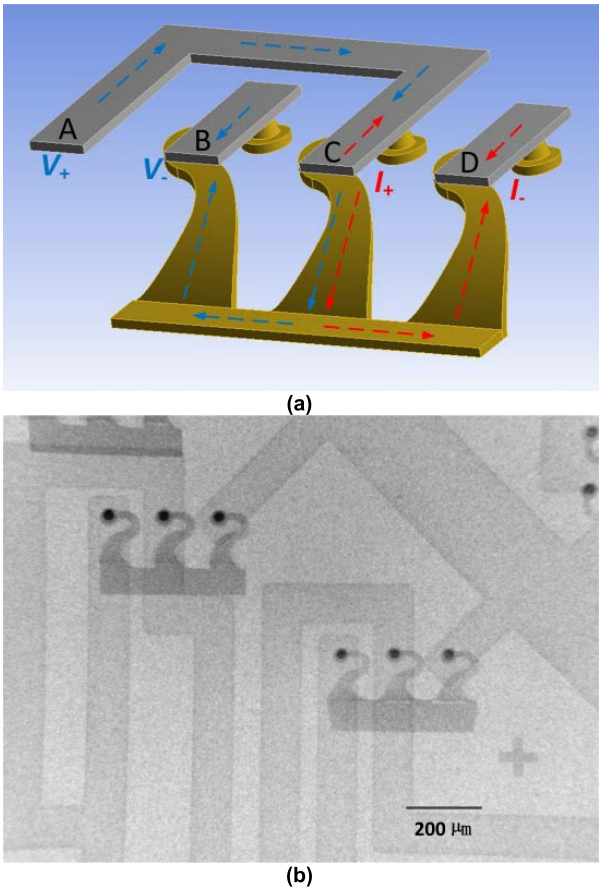

Fig. 12. (a) Schematic and (b) X-ray image of assembled four-point resistance measurement structures.

TABLE I
RESISTANCE CHARACTERIZATION FOR REMATABLE ASSEMBLY

	Average Resistance (mΩ)	Standard Deviation (mΩ)
After 1st assembly	103.21	4.06
After 10th assembly	105.99	4.40

TABLE II
RESISTANCE OF VARIOUS DAISY CHAIN DESIGNS

Daisy Chain Design	Number of MFIs	Average Resistance (Ω)	Standard Deviation (Ω)
C1	24	2.897	0.045
C2	18	2.115	0.025
C3	12	1.378	0.030

Fig. 15 shows three different daisy-chain lengths on the assembled test vehicle: daisy chains C1–C3 contained a total of 24 MFIs, 18 MFIs, and 12 MFIs, respectively. The measured resistance of daisy chains C1–C3 is 2.897, 2.115, and 1.378 Ω, respectively, as summarized in Table II.

Daisy chain C1 was used for current carrying capability measurement as well. The test setup is shown in Fig. 16. The

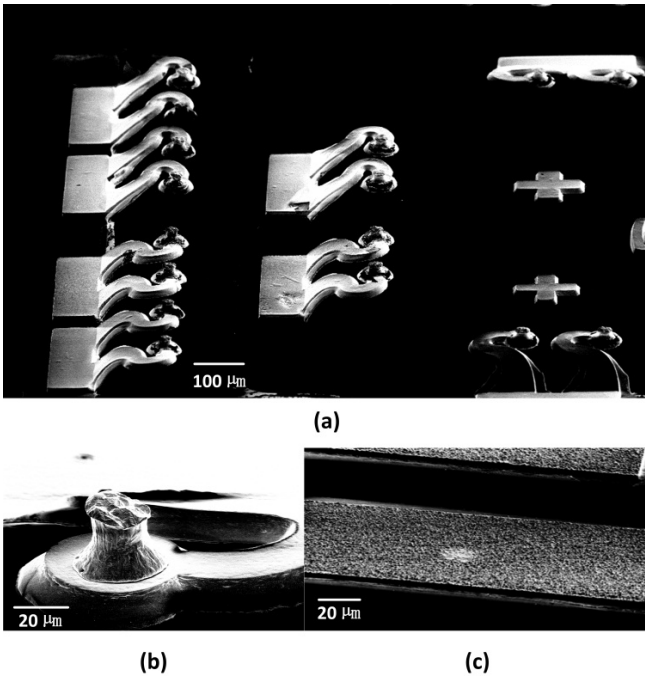

Fig. 13. (a) SEM images of Au–NiW MFIs, including (b) magnified image of the tip and (c) traces, which were repeatedly assembled on for ten times.

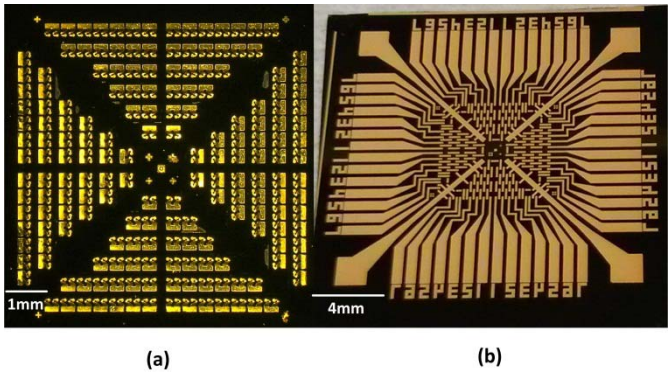

Fig. 14. Testbed with daisy chain measurement structures, which includes (a) chip with MFIs and (b) corresponding substrate, is used for yield and current carrying capability characterization.

assembled testbed was attached on an FR-4 test board with an opening at the center. An Agilent N6705B power analyzer was used as a power supply as well as for recording the input current and the output voltage of the testbed. Since a significant amount of heat is generated during the current carrying capability test, an air-cooled heat sink, RCK-ZAIO-92, designed for an Intel i7 processor was attached on top of the test vehicle through a TIM layer to avoid overheating. In addition, a thermal coupler was attached on the back side of the testbed through the opening of the test board to monitor the real-time temperature of the testbed.

For each test, the input current is increased from 10 mA to 1 A. After the first current ramp was accomplished, the testbed was cooled down for 20 min. Once the sample reached room temperature, approximately, a second current ramp was performed for comparison. The voltage and the corresponding

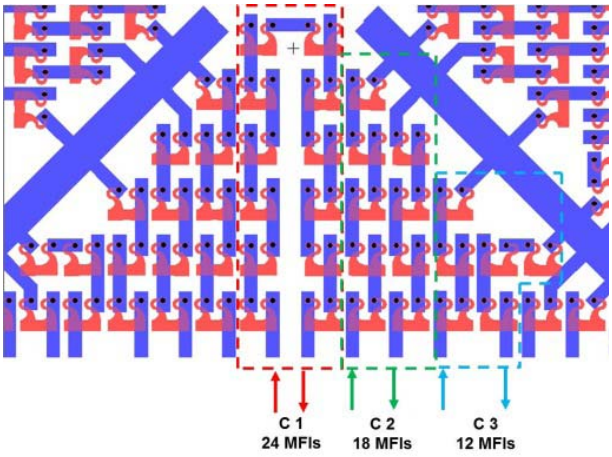

Fig. 15. Three daisy chain designs consisting of different number of MFIs—daisy chains C1–C3 contained 24, 18, and 12 MFIs, respectively.

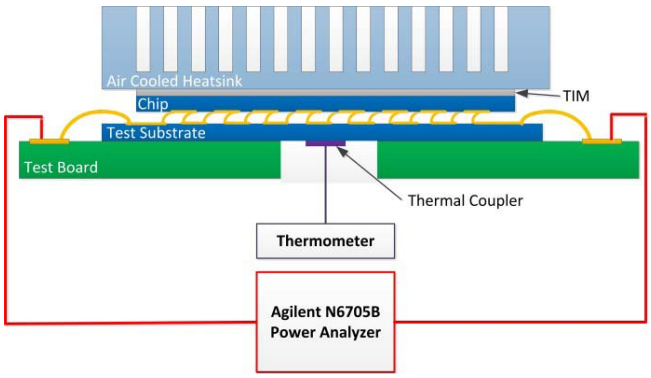

Fig. 16. Test setup used for current carrying capability test.

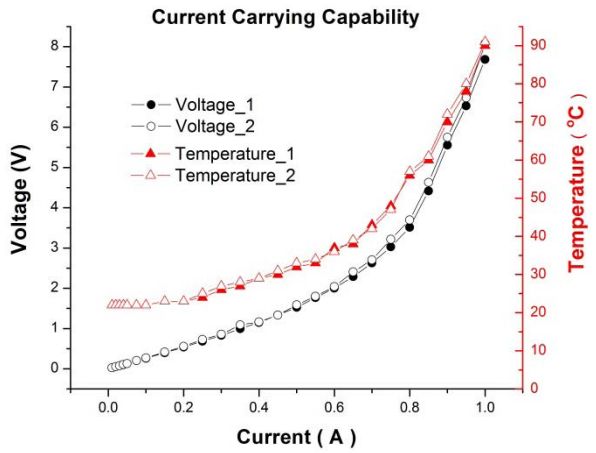

Fig. 17. Current–voltage and current–temperature curves of current carrying capability test performed on a testbed with daisy chain design.

temperature accompanied with the two current runs were recorded, as shown in Fig. 17.

At the beginning of each test, the voltage was linear with respect to the input current. The slope of the I–V curve is 2.89 Ω, which is the resistance of the daisy chain C1 at room temperature. This linear relationship remained until the current reached approximately 0.4 A, which coincides with

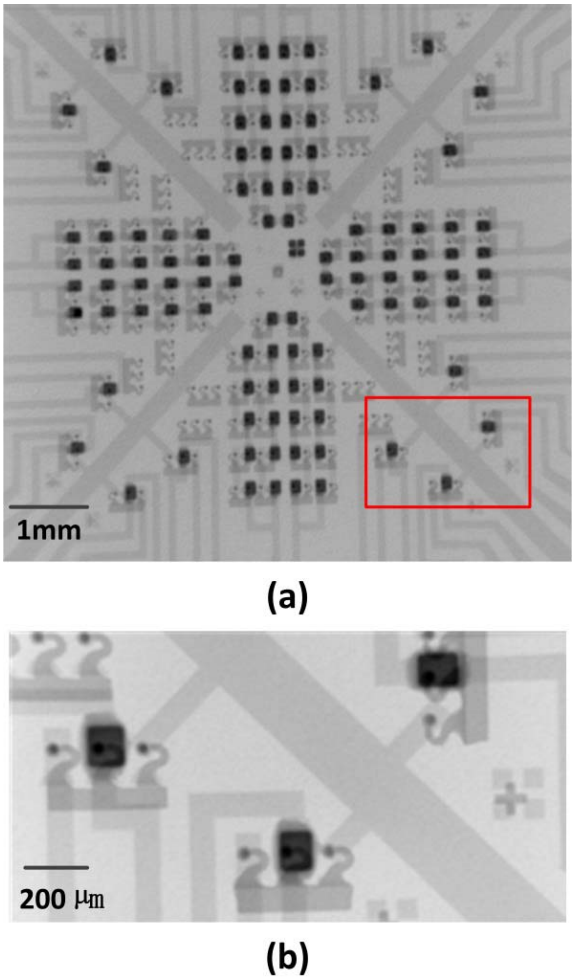

Fig. 18. X-ray images of the assembled chip with MFIs on a substrate with nonuniform-height pads: (a) overview and (b) four-point resistance measurement configuration.

the temperature of the assembled test vehicle reaching 30 °C. As the input current and power increases further, the voltage becomes nonlinear to input current, which indicates an increased daisy chain resistance. Such a resistance change is believed to be caused by the increased temperature, which is shown in Fig. 17 as well. The I–V curves of the two experiments are overlapped, which indicates that the MFIs can sustain an input current of 1 A.

IV. MFIs-Assisted Assembly on Nonplanar Substrate

In this section, temporary assembly on the nonplanar substrate is demonstrated using the testbed shown in Fig. 6(b). As noted previously, the pad-to-pad height difference on the substrate was 45 μm.

As shown in Fig. 18, the X-ray images following assembly indicate that the chip is well aligned with the substrate. The black dot on top of the MFIs is the truncated-cone tip, and the dark rectangular areas above the center-located MFIs are the high-profile pads, which are 48 μm tall as described previously.

Four-point resistance measurements of the assembled MFIs making contact to the high-profile pads are summarized

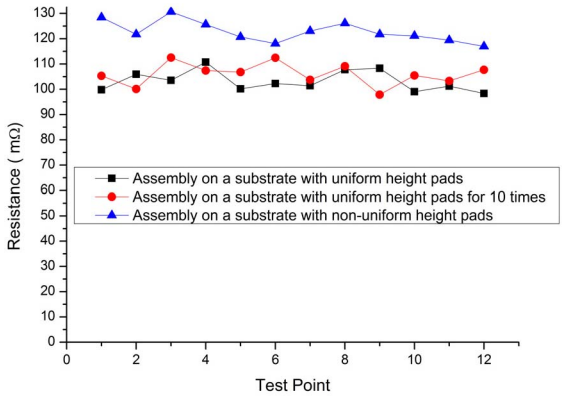

Fig. 19. Four-point resistance measurements of MFIs assembled on various test substrates.

in Fig. 19. The average resistance of the assembled MFI/high-profile pad combination is 122.81 mΩ with a standard deviation of 4.16 mΩ. The measured average resistance is 9.6 mΩ larger than the average resistance of the assembled MFI/low-profile pad combination reported in Section III and summarized in Table I. This increase in resistance can be attributed to both the thicker pad and the increased surface roughness described previously, which can increase the contact resistance.

V. Conclusion

Au–NiW MFIs with truncated cone tip were wafer-level batch fabricated and used to demonstrate rematable assembly on various substrates. Four-point resistance measurements were reported as well. The truncated cone tip enhances bonding pad scrubbing. In addition, daisy chain and current carrying capability measurements indicate that the Au–NiW MFIs form reliable interconnects and exhibit a large current carrying capability of 1 A. Finally, due to the large vertical range of motion, Au–NiW MFIs enable the assembly of a silicon chip onto a substrate with up to 45 μm surface variation.

Acknowledgment

The authors would like to thank Dr. K. Raj from Oracle and Dr. J. Mitchell for their valuable discussions and support.

References

[1] J. U. Knickerbocker *et al.*, "An advanced multichip module (MCM) for high-performance UNIX servers," *IBM J. Res. Develop.*, vol. 46, no. 6, pp. 779–804, Nov. 2002.

[2] J. E. Cunningham *et al.*, "Aligning chips face-to-face for dense capacitive and optical communication," *IEEE Trans. Adv. Packag.*, vol. 33, no. 2, pp. 389–397, May 2010.

[3] B. Banijamali, S. Ramalingam, K. Nagarajan, and R. Chaware, "Advanced reliability study of TSV interposers and interconnects for the 28nm technology FPGA," in *Proc. 61st ECTC*, May/Jun. 2011, pp. 285–290.

[4] J. E. Cunningham *et al.*, "Integration and packaging of a macrochip with silicon nanophotonic links," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 3, pp. 546–558, May/Jun. 2011.

[5] R. Chaware, K. Nagarajan, and S. Ramalingam, "Assembly and reliability challenges in 3D integration of 28nm FPGA die on a large high density 65nm passive interposer," in *Proc. 62nd ECTC*, May/Jun. 2012, pp. 279–283.

[6] F. M. Baez *et al.*, "Electrical design and performance of a multichip module on a silicon interposer," in *Proc. 21st EPEPS*, Oct. 2012, pp. 303–306.

[7] J. Warnock *et al.*, "Circuit and physical design of the zEnterprise EC12 microprocessor chips and multi-chip module," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 9–18, Jan. 2014.

[8] N. L. Tracy *et al.*, "Array sockets and connectors using MicroSpring technology," in *Proc. 26th IEEE/CPMT Int. Electron. Manuf. Technol. Symp.*, Oct. 2000, pp. 129–140.

[9] Y.-G. Kim, I. Mohammed, B.-S. Seol, and T.-G. Kang, "Wide area vertical expansion (WAVE) package design for high speed application: Reliability and performance," in *Proc. 51st ECTC*, May/Jun. 2001, pp. 54–62.

[10] R. Fillion, R. J. Wojnarowski, H. Cole, and G. Claydon, "On-wafer process for stress-free area array floating pads," in *Proc. Int. Symp. Microelectron.*, Oct. 2001, pp. 100–105.

[11] R. B. Marcus, "A new coiled microspring contact technology," in *Proc. 51st ECTC*, May/Jun. 2001, pp. 1227–1232.

[12] H. D. Thacker, M. S. Bakir, D. C. Keezer, K. P. Martin, and J. D. Meindl, "Compliant probe substrates for testing high pin-count chip scale packages," in *Proc. 52nd ECTC*, May 2002, pp. 1188–1193.

[13] L. Ma, Q. Zhu, T. Hantschel, D. K. Fork, and S. K. Sitaraman, "J-springs—Innovative compliant interconnects for next-generation packaging," in *Proc. 52nd ECTC*, May 2002, pp. 1359–1365.

[14] Q. Zhu, L. Ma, and S. K. Sitaraman, "β-Helix: A lithography-based compliant off-chip interconnect," *IEEE Trans. Compon. Packag. Technol.*, vol. 26, no. 3, pp. 582–590, Sep. 2003.

[15] M. S. Bakir *et al.*, "Sea of leads (SoL) ultrahigh density wafer-level chip input/output interconnections for gigascale integration (GSI)," *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2039–2048, Oct. 2003.

[16] S. Muthukumar *et al.*, "High-density compliant die-package interconnects," in *Proc. 56th ECTC*, May/Jun. 2006, pp. 1233–1238.

[17] K. Kacker, T. Sokol, and S. K. Sitaraman, "FlexConnects: A cost-effective implementation of compliant chip-to-substrate interconnects," in *Proc. 57th ECTC*, May/Jun. 2007, pp. 1678–1684.

[18] G. Spanier, C. Kruger, U. Schnakenberg, and W. Mokwa, "Platform for temporary testing of hybrid microsystems at high frequencies," *J. Microelectromech. Syst.*, vol. 16, no. 6, pp. 1367–1377, Dec. 2007.

[19] I. Shubin *et al.*, "Novel packaging with rematable spring interconnect chips for MCM," in *Proc. 59th ECTC*, May 2009, pp. 1053–1058.

[20] H. S. Yang and M. S. Bakir, "3D integration of CMOS and MEMS using mechanically flexible interconnects (MFI) and through silicon vias (TSV)," in *Proc. 60th ECTC*, Jun. 2010, pp. 822–828.

[21] H. S. Yang and M. S. Bakir, "Design, fabrication, and characterization of freestanding mechanically flexible interconnects using curved sacrificial layer," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 2, no. 4, pp. 561–568, Apr. 2012.

[22] M. S. Bakir *et al.*, "Revolutionary innovation in system interconnection: A new era for the IC," *Proc. SPIE*, vol. 7928, p. 792803, Feb. 2011.

[23] C. Zhang, H. S. Yang, and M. S. Bakir, "Gold passivated mechanically flexible interconnects (MFIs) with high elastic deformation," in *Proc. 62nd ECTC*, May/Jun. 2012, pp. 245–250.

[24] C. Zhang, H. S. Yang, and M. S. Bakir, "Highly elastic gold passivated mechanically flexible interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 10, pp. 1632–1639, Oct. 2013.

[25] C. Zhang, H. S. Yang, and M. S. Bakir, "Mechanically flexible interconnects with highly scalable pitch and large stand-off height for silicon interposer tile and bridge interconnection," in *Proc. 64th ECTC*, May 2014, pp. 13–19.

[26] C. Zhang, H. S. Yang, and M. S. Bakir, "Mechanically flexible interconnects (MFIs) with highly scalable pitch," *J. Micromech. Microeng.*, vol. 24, no. 5, p. 055024, 2014.

[27] H. S. Yang, C. Zhang, and M. S. Bakir, "Self-aligned silicon interposer tiles and silicon bridges using positive self-alignment structures and rematable mechanically flexible interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 11, pp. 1760–1768, Nov. 2014.

[28] C. Zhang, P. Thadesar, M. Zia, T. Sarvey, and M. S. Bakir, "Au-NiW mechanically flexible interconnects (MFIs) and TSV integration for 3D interconnects," in *Proc. IEEE 3D Syst. Integr. Conf. (3DIC)*, Cork, Republic of Ireland, Dec. 2014, pp. 1–4.

[29] H. S. Yang, C. Zhang, M. Zia, L. Zheng, and M. S. Bakir, "Interposer-to-interposer electrical and silicon photonic interconnection platform using silicon bridge," in *Proc. IEEE Photon. Soc. Opt. Interconnects Conf.*, Coronado, CA, USA, May 2014, pp. 71–72.

[30] M. Zia *et al.*, "A microfabricated electronic microplate platform for low-cost repeatable biosensing applications," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2015, pp. 29.4.1–29.4.4.

[31] M. Zia *et al.*, "Fabrication of and cell growth on 'silicon membranes' with high density TSVs for bio-sensing applications," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, Oct. 2015, pp. 1–4.
[32] Y. Zhang, Y. Zhang, T. Sarvey, C. Zhang, M. Zia, and M. Bakir, "Thermal isolation using air gap and mechanically flexible interconnects for heterogeneous 3-D ICs," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 1, pp. 31–39, Jan. 2016.
[33] S. Hinaga, "Effect of conductor surface roughness upon measured loss and extracted values of PCB laminate material dissipation factor," in *Proc. Tech. Conf. IPC Expo/APEX*, 2009, pp. 1–14.

Chaoqi Zhang received the B.S. degree in physics from Shandong University, Jinan, China, in 2005, the M.S. degree in microelectronics from Tsinghua University, Beijing, China, in 2008, and the Ph.D. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2015.

He is currently a Senior Hardware Engineer with the Fabric Silicon and Optical Interconnects Group, Oracle, where he is involved in advanced integration and packaging for a silicon-photonic device and system. He has coauthored over 20 articles in refereed journals and conference proceedings.

Dr. Zhang was a recipient of the 2014 IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY Best Paper Award for advanced packaging.

Hyung Suk Yang received the B.S. degree (Hons.) in computer engineering and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA.

While at the Georgia Institute of Technology, his research focused on 3-D heterogeneous integration using novel microfabricated interconnect technologies. He is the author or coauthor of 15 journal publications and conference proceedings.

Dr. Yang is a co-recipient of the 2009 and 2010 SRC TECHCON Best in Session Paper Award, the 2009 IMAPS Best Student Paper Award, and the 2009 IMAPS Best in Session Paper Award. He is a recipient of the Intel Corporation Ph.D. Fellowship for 2011–2012. In 2014, he received the Best Paper Award of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY in the area of advanced packaging.

Hiren D. Thacker received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from Georgia Institute of Technology, Atlanta, GA, USA, in 2000, 2002, and 2006, respectively.

He is currently a Principal Engineer with the Networking Division, Oracle Corporation, San Diego, CA, USA, where he is responsible for packaging of high-speed silicon photonic subsystems and networking ASICs. Prior to joining Sun/Oracle, he was a Research and Development MEMS Engineer at NanoNexus Inc., San Jose, CA, USA, where he helped commercialize wafer-scale stressed-metal MEMS interconnects for IC probing. He has coauthored over 75 articles in refereed journals and conference proceedings, and holds over 20 U.S. patents.

Ivan Shubin received the M.S. degree from the Moscow Institute of Physics and Technology, Moscow, Russia, in 1988, and the Ph.D. degree in electrical engineering from the Center for Research and Education in Optics and Lasers, School of Optics, University of Central Florida, Orlando, FL, USA, in 2001.

From 2001 to 2007, he was a Senior Engineer with Optium/Finisar, Orlando, FL, USA, and then a Project Scientist with the University of California at San Diego, La Jolla, CA, USA. Since 2007, he has been with Oracle Corporation, San Diego, CA, USA, where he is a Senior Principal Hardware Engineer involved in advanced packaging solutions and platforms for electronic, optoelectronic, and MEMS applications, wafer scale packaging, 3-D integration, and novel photonic components. He has authored and coauthored over 100 technical papers and conference presentations.

John E. Cunningham received the B.S. degree from the University of Tennessee, Knoxville, TN, USA, and the M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign, Champaign, IL, USA, all in physics.

He is a veteran Research Scientist with over 25 years of University, Bell Labs, Sun Labs of Sun Microsystems/Oracle, and start-up experience in the area of optoelectronic and semiconductor devices and packaging used within optical networks. Since joining Sun Labs, he has led advanced packaging initiatives to develop Inter-chip Proximity Communication and involved on Si nanophotonics solutions for data communications within computers. Before joining Sun Microsystems, he served as the Chief Scientist at Aralight, where he developed products based on the hybrid integration of vertical cavity surface emitting lasers and photodetectors with CMOS, a technology he co-developed at Bell Laboratories. While at Bell Laboratories, he also pioneered eight world records on various types of quantum mechanically engineered devices and materials; coauthored over 360 journal papers including some with Nobel Prize Laureates; and holds 40 U.S. patents. Before joining Bell Laboratories, has was a member of the Research Faculty with the Physics Department, University of Illinois at Urbana–Champaign, where he initiated the first Metals Molecular Beam Epitaxy. He is currently a Distinguished Engineer at Sun Labs, Oracle Corporation, San Diego, CA, USA, and is the Principal Lead of the Advanced Packaging Group while simultaneously serving as a Co-Principal Investigator for the DARPA UNIC Project.

Muhannad S. Bakir (SM'12) received the B.E.E. degree from Auburn University, Auburn, AL, USA, in 1999, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2000 and 2003, respectively.

He is currently a Professor with the School of Electrical and Computer Engineering, Georgia Institute of Technology. His current research interests include 3-D electronic system integration, advanced cooling and power delivery for 3-D systems, biosensors and their integration with CMOS circuitry, and nanofabrication technology.

Dr. Bakir is a recipient of the 2013 Intel Early Career Faculty Honor Award, the 2012 DARPA Young Faculty Award, and the 2011 IEEE CPMT Society Outstanding Young Engineer Award. He was an Invited Participant in the 2012 National Academy of Engineering Frontiers of Engineering Symposium. In 2015, he was elected by the IEEE CPMT Society to serve as a Distinguished Lecturer for a four-year term. He and his research group have received over 20 conference and student paper awards, including five from the IEEE Electronic Components and Technology Conference, four from the IEEE International Interconnect Technology Conference, and one from the IEEE Custom integrated Circuits Conference. His group was awarded the 2014 Best Paper of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY in the area of advanced packaging. He is an Editor of IEEE TRANSACTIONS ON ELECTRON DEVICES and an Associate Editor of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY.